

Trusted Firmware-A Tech Forum

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Trusted Firmware-A Testing Framework Overview

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Topics

- Testing framework architecture
- Platform ports
- Tests
- Improvement areas

Introduction

- Suite of bare metal tests to exercise the Trusted Firmware-A (TF-A) features from the Normal World (EL2 or EL1)
- Run-to-completion model executing on the boot CPU
- Functional testing without dependency on a Rich OS
- Interacts with TF-A through its SMC interface

Building blocks

- Core framework
- Drivers: GIC, UART, flash, timers, etc
- Interrupts: SGIs #0 to #7 as NS interrupts, SGI #7 as wake IRQ
- Logging: non-volatile memory, UART console
- Libraries: events, irq, power mgmt, inter-CPU communication, IO
- Makefiles and XML files
- Platform ports
- Tests under tftf/tests
- Test images: TFTF test binary, firmware update, SPM, SPM-MM
- Test database: tests_list.c (build artifact)

Available Tests

- Framework validation tests
- Runtime services tests
- CPU extensions tests
- Firmware update tests
- Template tests
- Performance tests
- Miscellaneous tests

```
Supported Tests:
arm-state-switch
boot-req
cpu-extensions
debugfs
el3-power-state
extensive
fwu
manual
manual-shutdown
performance
pmu-leakage
psci
psci-extensive
quark
reboot
reboot_reset2
runtime-instrumentation
sdei
single-fault
smc
spm
spm-mm
standard
tegral94
template
tftf-validation
tsp
uncontainable
unstable
xlat-v2
```

```
***** Summary *****
> Test suite 'Framework Validation'                               Passed
> Test suite 'Timer framework Validation'                         Passed
> Test suite 'Query runtime services'                             Passed
> Test suite 'PSCI Version'                                       Passed
> Test suite 'PSCI Affinity Info'                                 Passed
> Test suite 'CPU Hotplug'                                         Passed
> Test suite 'PSCI CPU Suspend'                                   Passed
> Test suite 'PSCI STAT'                                           Passed
> Test suite 'PSCI NODE_HW_STATE'                                 Passed
> Test suite 'PSCI Features'                                       Passed
> Test suite 'PSCI MIGRATE_INFO_TYPE'                             Passed
> Test suite 'PSCI mem_protect_check'                             Passed
> Test suite 'SDEI'                                               Passed
> Test suite 'Runtime Instrumentation Validation'                 Passed
> Test suite 'IRQ support in TSP'                                  Passed
> Test suite 'TSP handler standard functions result test'         Passed
> Test suite 'Stress test TSP functionality'                       Passed
> Test suite 'EL3 power state parser validation'                   Passed
> Test suite 'State switch'                                        Passed
> Test suite 'CPU extensions'                                       Passed
> Test suite 'ARM_ARCH_SVC'                                         Passed
> Test suite 'Performance tests'                                   Passed
> Test suite 'SMC calling convention'                               Passed
> Test suite 'PSA FF-A Version'                                     Passed
> Test suite 'PSA FF-A Direct messaging'                           Passed
> Test suite 'PSA FF-A features'                                   Passed
> Test suite 'PMU Leakage'                                         Passed
> Test suite 'DebugFS'                                             Passed
*****
Tests Skipped : 57
Tests Passed  : 43
Tests Failed  : 0
Tests Crashed : 0
Total tests   : 100
*****
NOTICE: Exiting tests.
```

Available platforms

Vendor	Platform name
Arm	FVP, Juno, RD-N1-Edge, SGI575
HiSilicon	Hikey960
NVIDIA	Tegra194, Tegra186, Tegra210

Platform port requirements

- Mandatory drivers
 - GIC
 - Watchdog timer
 - System timer
 - Non-volatile memory or DRAM region for logging
- Crash console
- Power domain tree
- Physical to logical CPU ID
- Platform defines: stack size, cluster and core count, image base, IRQ
- List of tests to skip (optional)

Implementing tests

- **Prologue:** `typedef test_result_t (*test_function_t) (void)`
 - Main entry function running on boot CPU
 - Should run to completion
 - Should return the test status to the framework
- **Build**
 - Tests should be added to an existing or new `.mk` under `tftf/tests`
 - Tests should be added to corresponding `.xml` under `tftf/tests`
 - Names for `.mk` and `.xml` must match
 - Generate `tftf.bin` with the new tests
- **Sample tests**
 - `tftf/tests/template_tests`

How to enable or disable tests?

- Enable tests

export CROSS_COMPILE=<toolchain> PLAT=<platform> TESTS=<test suite> tftf

- Disable failing tests from tests_to_skip.txt

```
# Tegra194 platforms enter system suspend only from the boot core
PSCI System Suspend Validation/system suspend from all cores

# Tegra194 platforms do not support CPU suspend with PSTATE_TYPE_POWERDOWN
PSCI STAT/Stats test cases for CPU OFF
PSCI STAT/Stats test cases after system suspend

# Tegra194 platforms do not support memory mapped timers
Boot requirement tests
```

Improvement areas

- Position independent execution
- One test binary for all platforms
- Support for running the test image as a NS VM
- Interactive shell
- Dynamic installation of tests
- More tests to improve code coverage
- More platforms

References

- <https://trustedfirmware-a-tests.readthedocs.io/en/latest/about/index.html>
- https://trustedfirmware-a-tests.readthedocs.io/en/latest/getting_started/index.html
- <https://trustedfirmware-a-tests.readthedocs.io/en/latest/design.html>
- <https://trustedfirmware-a-tests.readthedocs.io/en/latest/porting/index.html>
- <https://trustedfirmware-a-tests.readthedocs.io/en/latest/implementing-tests.html>

Questions?